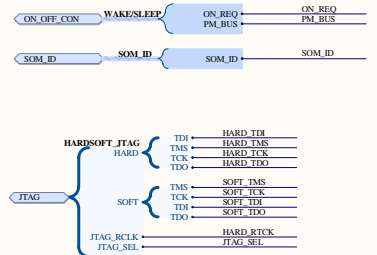


PCB1
SOM03 Blank PCB
Printed Circuit Board (Bare)

Title		
Size	Number	Revision
A3		
Date:	23/09/2011	Sheet of
File:	C:\SRKHSOM03 - XC3S1600E\SOM03	SchDoc By:



		CNI FPGA		TOP COMP SIDE		BOTTOM SOLDER SIDE			
JTAG_TDI	HARD_TDI	1	JTAG_TDI	2	HARD_TDI	JTAG_TDI	2	JTAG_TDI	JTAG_TDI
JTAG_TCK	HARD_TCK	4	JTAG_TCK	5	HARD_TCK	JTAG_TCK	5	JTAG_TCK	JTAG_TCK
SOM_ID	ON_REQ	7	SOM_ID	8	ON_REQ	JTAG_SEL	10	JTAG_SEL	JTAG_SEL
ENET_Ap	ENET_Ap	9	ENET_Ap	9	ENET_Ap	GND	10	GND	GND
ENET_Bp	ENET_Bp	10	ENET_Bp	10	ENET_Bp	FPGA_I0p	11	FPGA_I0p	ENET_Bp
ENET_Cp	ENET_Cp	11	ENET_Cp	11	ENET_Cp	FPGA_I0n	12	FPGA_I0n	ENET_Cp
ENET_Dp	ENET_Dp	12	ENET_Dp	12	ENET_Dp	FPGA_I0p	13	FPGA_I0p	ENET_Dp
ENET_Dn	ENET_Dn	13	ENET_Dn	13	ENET_Dn	FPGA_I0n	14	FPGA_I0n	ENET_Dn
GND	GND	21	GND	21	GND	GND	22	GND	GND
+B	+B	22	+B	22	+B	+B	23	+B	+B
US2B_1_VBUS	PWR_OUT11	25	US2B_1_VBUS	25	PWR_SW	PWR_SW	26	PWR_SW	US2B_2_VBUS
US2B_1_DP	PWR_OUT11	26	US2B_1_DP	26	PWR_SW	PWR_SW	27	PWR_SW	US2B_2_VBUS
US2B_1_Dn	FPGA_I0p	28	US2B_1_Dn	28	FPGA_I0p	FPGA_I0p	29	FPGA_I0p	US2B_2_DP
US2B2_DP	FPGA_I0n	30	US2B2_DP	30	FPGA_I0n	FPGA_I0n	31	FPGA_I0n	US2B_2_Dn
US2B2_Dn	GND	31	US2B2_Dn	31	GND	GND	32	GND	GND
US2B3_DP	FPGA_I0p	32	US2B3_DP	32	FPGA_I0p	FPGA_I0p	33	FPGA_I0p	US2B_3_DP
US2B3_Dn	FPGA_I0n	33	US2B3_Dn	33	FPGA_I0n	FPGA_I0n	34	FPGA_I0n	US2B_3_Dn
US2B3_VBUS	PWR_OUT11	34	US2B3_VBUS	34	PWR_SW	PWR_SW	35	PWR_SW	US2B_3_VBUS
US2B3_DP	PWR_OUT11	35	US2B3_DP	35	PWR_SW	PWR_SW	36	PWR_SW	US2B_3_DP
US2B3_Dn	FPGA_I0p	36	US2B3_Dn	36	FPGA_I0p	FPGA_I0p	37	FPGA_I0p	GND
US2B3_VBUS	FPGA_I0n	37	US2B3_VBUS	37	FPGA_I0n	FPGA_I0n	38	FPGA_I0n	GND
UART1_RTS	SOFT_TSD	38	UART1_RTS	38	SOFT_TSD	PM_BUS	39	PM_BUS	UART2_TXD
UART1_TXD	SOFT_TMS	39	UART1_TXD	39	SOFT_TMS	SOFT_TDO	40	SOFT_TDO	UART2_RTS
UART1_RXD	SOFT_TMS	40	UART1_RXD	40	SOFT_TMS	SOFT_TMS	41	SOFT_TMS	UART2_RXD
UART1_CTS	SOFT_TDI	41	UART1_CTS	41	SOFT_TDI	SOFT_TDI	42	SOFT_TDI	UART2_CTS
GND	SOFT_TCK	42	GND	42	SOFT_TCK	SOFT_TCK	43	SOFT_TCK	GND
SPI_TXD	FPGA_I0p	56	SPI_TXD	56	FPGA_I0p	FPGA_I0p	57	FPGA_I0p	I2S_CS
SPI_CLK	GND	57	SPI_CLK	57	GND	GND	58	GND	I2S_CDOUT
SPI_CS	FPGA_I0n	58	SPI_CS	58	FPGA_I0n	FPGA_I0n	59	FPGA_I0n	I2S_CLK
SPI_RXD	FPGA_I0p	59	SPI_RXD	59	FPGA_I0p	FPGA_I0p	60	FPGA_I0p	I2S_CIN
SPI_TXD	FPGA_I0n	60	SPI_TXD	60	FPGA_I0n	FPGA_I0n	61	FPGA_I0n	I2S_LCLK
SP2_RXD	FPGA_I0p	61	SP2_RXD	61	FPGA_I0p	FPGA_I0p	62	FPGA_I0p	I2S_SCLK
SP2_CLK	FPGA_I0n	62	SP2_CLK	62	FPGA_I0n	FPGA_I0n	63	FPGA_I0n	I2S_SIN
GND	FPGA_I0p	63	GND	63	FPGA_I0p	FPGA_I0p	64	FPGA_I0p	I2S_SDOUT
+B	GND	77	+B	77	GND	GND	78	GND	+B
+B	+B	78	+B	78	+B	+B	79	+B	+B
+B	+B	79	+B	79	+B	+B	80	+B	+B
+B	+B	80	+B	80	+B	+B	81	+B	+B
BUS_A0	FPGA_I0p	81	BUS_A0	81	FPGA_I0p	FPGA_I0p	82	FPGA_I0p	BUS_D0
BUS_A1	FPGA_I0n	82	BUS_A1	82	FPGA_I0n	FPGA_I0n	83	FPGA_I0n	BUS_D1
BUS_A2	FPGA_I0p	83	BUS_A2	83	FPGA_I0p	FPGA_I0p	84	FPGA_I0p	BUS_D2
BUS_A3	FPGA_I0n	84	BUS_A3	84	FPGA_I0n	FPGA_I0n	85	FPGA_I0n	BUS_D3
BUS_A4	FPGA_I0p	85	BUS_A4	85	FPGA_I0p	FPGA_I0p	86	FPGA_I0p	BUS_D4
BUS_A5	FPGA_I0n	86	BUS_A5	86	FPGA_I0n	FPGA_I0n	87	FPGA_I0n	BUS_D5
BUS_A6	FPGA_I0p	87	BUS_A6	87	FPGA_I0p	FPGA_I0p	88	FPGA_I0p	BUS_D6
BUS_A7	FPGA_I0n	88	BUS_A7	88	FPGA_I0n	FPGA_I0n	89	FPGA_I0n	BUS_D7
BUS_A8	FPGA_I0p	89	BUS_A8	89	FPGA_I0p	FPGA_I0p	90	FPGA_I0p	BUS_D8
BUS_A9	FPGA_I0n	90	BUS_A9	90	FPGA_I0n	FPGA_I0n	91	FPGA_I0n	BUS_D9
BUS_A10	FPGA_I0p	91	BUS_A10	91	FPGA_I0p	FPGA_I0p	92	FPGA_I0p	BUS_D10
BUS_A11	FPGA_I0n	92	BUS_A11	92	FPGA_I0n	FPGA_I0n	93	FPGA_I0n	BUS_D11
BUS_A12	FPGA_I0p	93	BUS_A12	93	FPGA_I0p	FPGA_I0p	94	FPGA_I0p	BUS_D12
BUS_A13	FPGA_I0n	94	BUS_A13	94	FPGA_I0n	FPGA_I0n	95	FPGA_I0n	BUS_D13
BUS_A14	FPGA_I0p	95	BUS_A14	95	FPGA_I0p	FPGA_I0p	96	FPGA_I0p	BUS_D14
BUS_A15	FPGA_I0n	96	BUS_A15	96	FPGA_I0n	FPGA_I0n	97	FPGA_I0n	BUS_D15
GND	FPGA_I0p	116	GND	116	FPGA_I0p	FPGA_I0p	117	FPGA_I0p	GND
BUS_A16	FPGA_I0n	117	BUS_A16	117	FPGA_I0n	FPGA_I0n	118	FPGA_I0n	BUS_CSD
BUS_A17	FPGA_I0p	118	BUS_A17	118	FPGA_I0p	FPGA_I0p	119	FPGA_I0p	BUS_CSI
BUS_A18	FPGA_I0n	119	BUS_A18	119	FPGA_I0n	FPGA_I0n	120	FPGA_I0n	BUS_CSE
BUS_A19	FPGA_I0p	120	BUS_A19	120	FPGA_I0p	FPGA_I0p	121	FPGA_I0p	BUS_INT0
BUS_A20	FPGA_I0n	121	BUS_A20	121	FPGA_I0n	FPGA_I0n	122	FPGA_I0n	BUS_INT1
BUS_DMACK	FPGA_I0p	122	BUS_DMACK	122	FPGA_I0p	FPGA_I0p	123	FPGA_I0p	BUS_AWE
BUS_DMARQ	FPGA_I0n	123	BUS_DMARQ	123	FPGA_I0n	FPGA_I0n	124	FPGA_I0n	BUS_WAIT
BUS_AADV	FPGA_I0p	124	BUS_AADV	124	FPGA_I0p	FPGA_I0p	125	FPGA_I0p	BUS_CLK
BUS_AOE	FPGA_I0n	125	BUS_AOE	125	FPGA_I0n	FPGA_I0n	126	FPGA_I0n	+B
+B	FPGA_I0p	126	+B	126	FPGA_I0p	FPGA_I0p	127	FPGA_I0p	+B
+B	+B	127	+B	127	+B	+B	128	+B	+B
+B	+B	128	+B	128	+B	+B	129	+B	+B
FXB1ANK	FPGA_I0p	129	FXB1ANK	129	FPGA_I0p	FPGA_I0p	130	FPGA_I0p	SD1_DAT0
PXDAT0	FPGA_I0n	130	PXDAT0	130	FPGA_I0n	FPGA_I0n	131	FPGA_I0n	SD1_DAT1
PXDAT1	FPGA_I0p	131	PXDAT1	131	FPGA_I0p	FPGA_I0p	132	FPGA_I0p	SD1_DAT2
PXDAT2	FPGA_I0n	132	PXDAT2	132	FPGA_I0n	FPGA_I0n	133	FPGA_I0n	SD1_DAT3
PXDAT3	FPGA_I0p	133	PXDAT3	133	FPGA_I0p	FPGA_I0p	134	FPGA_I0p	SD1_CMD
PXDAT4	FPGA_I0n	134	PXDAT4	134	FPGA_I0n	FPGA_I0n	135	FPGA_I0n	SD1_CLK
PXDAT5	FPGA_I0p	135	PXDAT5	135	FPGA_I0p	FPGA_I0p	136	FPGA_I0p	SD1_CD
PXDAT6	FPGA_I0n	136	PXDAT6	136	FPGA_I0n	FPGA_I0n	137	FPGA_I0n	SD1_PWR
PXDAT7	FPGA_I0p	137	PXDAT7	137	FPGA_I0p	FPGA_I0p	138	FPGA_I0p	SD2_DAT0
PXDAT8	FPGA_I0n	138	PXDAT8	138	FPGA_I0n	FPGA_I0n	139	FPGA_I0n	SD2_DAT1
PXDAT9	FPGA_I0p	139	PXDAT9	139	FPGA_I0p	FPGA_I0p	140	FPGA_I0p	SD2_DAT2
PXDAT10	FPGA_I0n	140	PXDAT10	140	FPGA_I0n	FPGA_I0n	141	FPGA_I0n	SD2_DAT3
PXDAT11	FPGA_I0p	141	PXDAT11	141	FPGA_I0p	FPGA_I0p	142	FPGA_I0p	SD2_CMD
PXDAT12	FPGA_I0n	142	PXDAT12	142	FPGA_I0n	FPGA_I0n	143	FPGA_I0n	SD2_CLK
PXDAT13	FPGA_I0p	143	PXDAT13	143	FPGA_I0p	FPGA_I0p	144	FPGA_I0p	SD2_CD
PXDAT14	FPGA_I0n	144	PXDAT14	144	FPGA_I0n	FPGA_I0n	145	FPGA_I0n	SD2_PWR
PXDAT15	FPGA_I0p	145	PXDAT15	145	FPGA_I0p	FPGA_I0p	146	FPGA_I0p	DPDVI_HPD
PXDAT16	FPGA_I0n	146	PXDAT16	146	FPGA_I0n	FPGA_I0n	147	FPGA_I0n	DPDVI_CLK
PXDAT17	FPGA_I0p	147	PXDAT17	147	FPGA_I0p	FPGA_I0p	148	FPGA_I0p	DPDVI_n0
PXDAT18	FPGA_I0n	148	PXDAT18	148	FPGA_I0n	FPGA_I0n	149	FPGA_I0n	GND
PXDAT19	FPGA_I0p	149	PXDAT19	149	FPGA_I0p	FPGA_I0p	150	FPGA_I0p	DPDVI_p0
PXDAT20	FPGA_I0n	150	PXDAT20	150	FPGA_I0n	FPGA_I0n	151	FPGA_I0n	DPDVI_n1
PXDAT21	FPGA_I0p	151	PXDAT21	151	FPGA_I0p	FPGA_I0p	152	FPGA_I0p	DPDVI_p1
PXDAT22	FPGA_I0n	152	PXDAT22	152	FPGA_I0n	FPGA_I0n	153	FPGA_I0n	DPDVI_n2
PXDAT23	FPGA_I0p	153	PXDAT23	153	FPGA_I0p	FPGA_I0p	154	FPGA_I0p	DPDVI_p2
PDCLK	FPGA_I0n	154	PDCLK	154	FPGA_I0n	FPGA_I0n	155	FPGA_I0n	GND
PMHS	FPGA_I0p	155	PMHS	155	FPGA_I0p	FPGA_I0p	156	FPGA_I0p	DPDVI_n2
PMVS	FPGA_I0n	156	PMVS	156	FPGA_I0n	FPGA_I0n	157	FPGA_I0n	GND
+B	FPGA_I0p	157	+B	157	FPGA_I0p	FPGA_I0p	158	FPGA_I0p	DPDVI_CLKp
+B	+B	158	+B	158	+B	+B	159	+B	DPDVI_CLKn
+B	+B	159	+B	159	+B	+B	160	+B	GND
+B1	+B1	160	+B1	160	+B1	+B1	161	+B1	GND

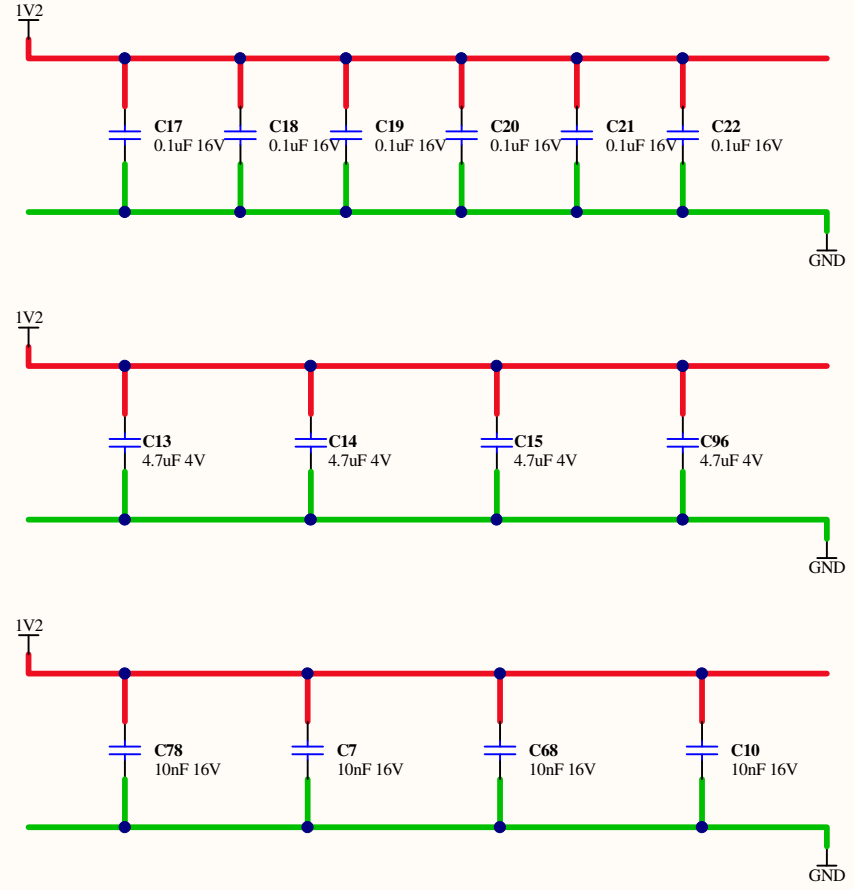
SOM PIN DESCRIPTIONS:


SERVICES:

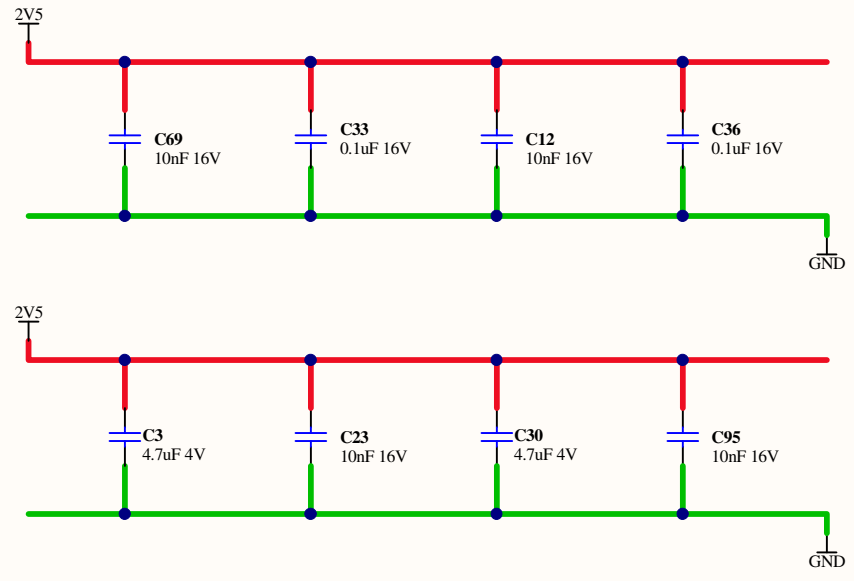
- 18x 4.5V TO 5.5V POWER PINS (5.4MAPS)
- 140x SINGLE ENDED 3.3V IO
- 13x DIFFERENTIAL PAIRS
- 11x SINGLE ENDED GLOBAL CLOCKS
- 1x DIFFERENTIAL GLOBAL CLOCK
- 4x 5VDC 600mA POWER OUTPUTS (ie USB PORT POWER)
- 2x 3.3VDC 600mA POWER OUTPUTS (ie SD CARD POWER)
- PLUG PACK DETECT/MONITOR (PMBUS)
- SOM ON/OFF CONTROL (ON REQ)
- SOM ID ROM (SOM ID)
- HARD JTAG WITH ADAPTIVE CLOCKING OPTION
- SOM JTAG CONTROLLER DETECT AND BUS REQUEST (JTAG SEL)


POWER HANDLING CAPACITY
MAX VOLTAGE PER PIN: 25V
MAX CURRENT PER PIN: 0.3A
NUMBER OF POWER PINS: GND x 19 + B x 18
MAX MODULE POWER: 27W (5V @ 5.4A)

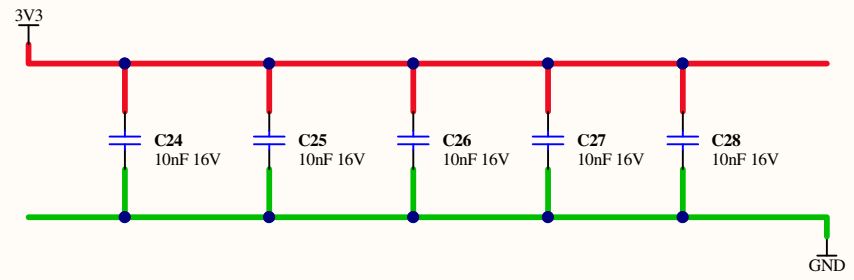
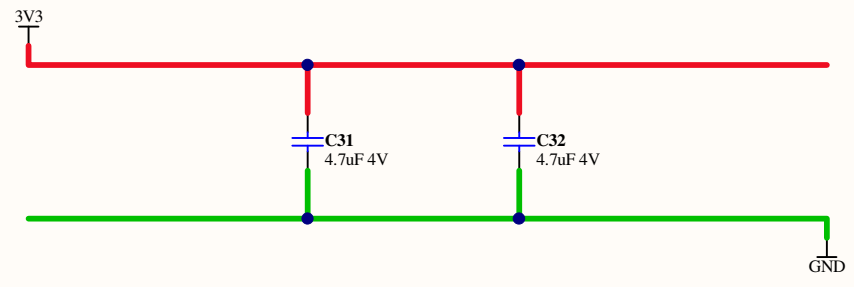
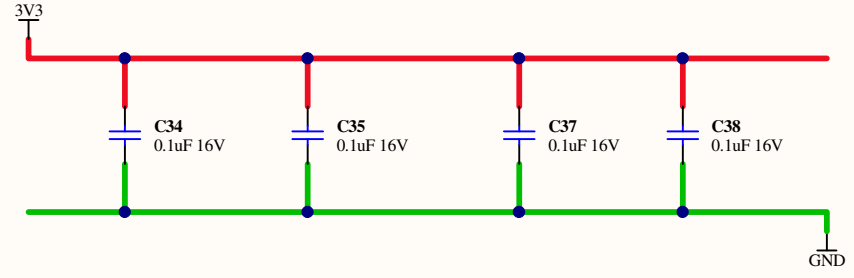
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Sheet Title FPGA Bypass 2V5		<i>Altium Limited</i> 3 Minna Close Belrose NSW 2085 Australia	
Project Title SOM02			
Size: A4	Assy: TBA		
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 3 of 13	
File: FPGA_Bypass_FPGA_1V2.SchDoc			

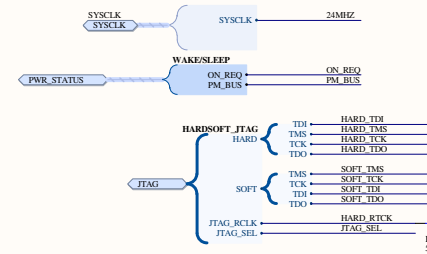


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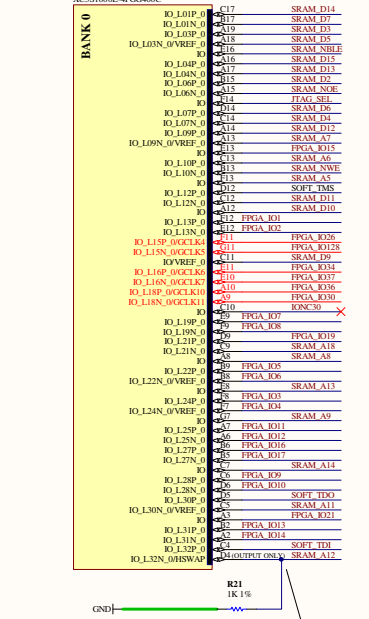
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Project Title SOM02			
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 5 of 13	
File: FPGA_Bypass FPGA_3V3.SchDoc			

SRAM - 64K/256K x 16

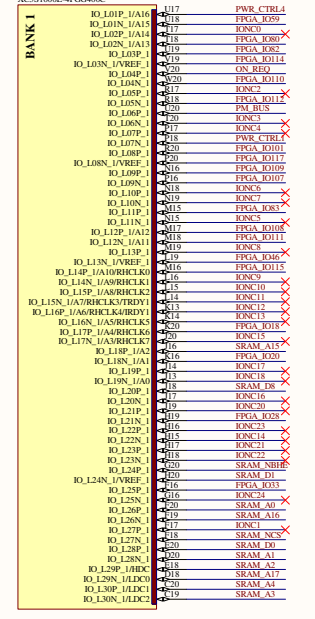


GCLK0
FPGA SYSTEM CLOCK IS ON GLOBAL CLOCK @ 24MHZ

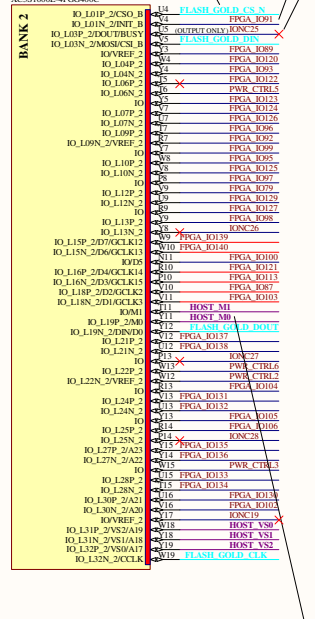
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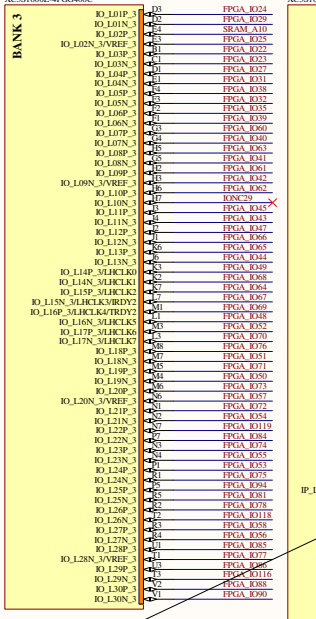
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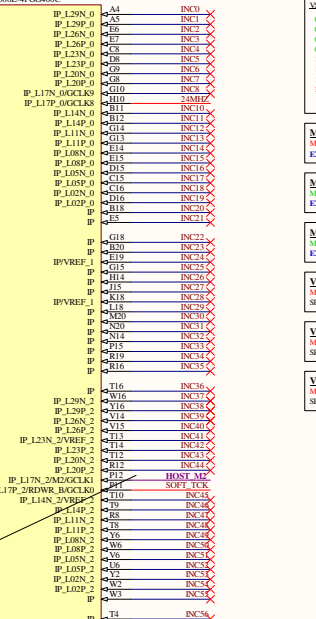
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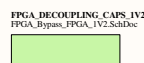
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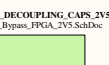
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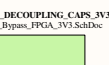
1V2



2V5

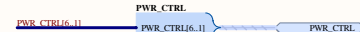


3V3

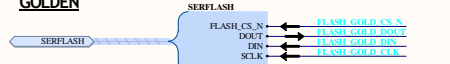


FPGA WILL ATTEMPT SPI BOOT THREE TIMES (UG312-P327)

NOTE:
INT B ASSERTS DURING CONFIG.
DOUT OSCILLATES DURING CONFIG.



XILINX MULTIBOOT COMPATIBLE GOLDEN



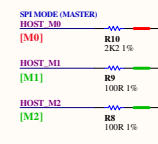
XC6SLX1600E MODE PIN CONFIGURATIONS

M0	M1	M2	FUNCTION
0	0	0	PLATFORM FLASH MODE
0	0	1	SPI MASTER (MASTER)
0	1	0	BYTE PARALLEL INTERFACE
0	1	1	INTERNAL MASTER SPI FLASH
1	0	0	<RESERVED>
1	0	1	JTAG MODE
1	1	0	SLAVE PARALLEL
1	1	1	SLAVE SERIAL

(M0)
M0 = H
INTERNAL PULL UP BY HSWAP PRIOR TO CONFIGURATION (UG312-P36)

XC6SLX1600E SPI MODE CONFIGURATIONS

M0	M1	M2	FUNCTION
0	0	0	<RESERVED>
0	0	1	<RESERVED>
0	1	0	<RESERVED>
0	1	1	(0x0) STANDARD READ
1	1	0	(0x0) READ ARBITRARY
1	1	1	(0x0) SPI FAST READ



M0 (INT PULL UP VIA HSWAP) MUST BE PULLED HIGH DURING CONFIG EXT SPI BOOT MODE (MASTER)

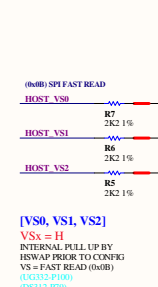
M1 (INT PULL UP VIA HSWAP) MUST BE PULLED LOW DURING CONFIG EXT SPI BOOT MODE (MASTER)

M2 (INT PULL UP VIA HSWAP) MUST BE PULLED LOW DURING CONFIG EXT SPI BOOT MODE (MASTER)

VS0 SPI ACCESS SPEED (INT PULL UP VIA HSWAP) SPI SET TO FAST (0x0) (VCCO-2)

VS1 SPI ACCESS SPEED (INT PULL UP VIA HSWAP) SPI SET TO FAST (0x0) (VCCO-2)

VS2 SPI ACCESS SPEED (INT PULL UP VIA HSWAP) SPI SET TO FAST (0x0) (VCCO-2)



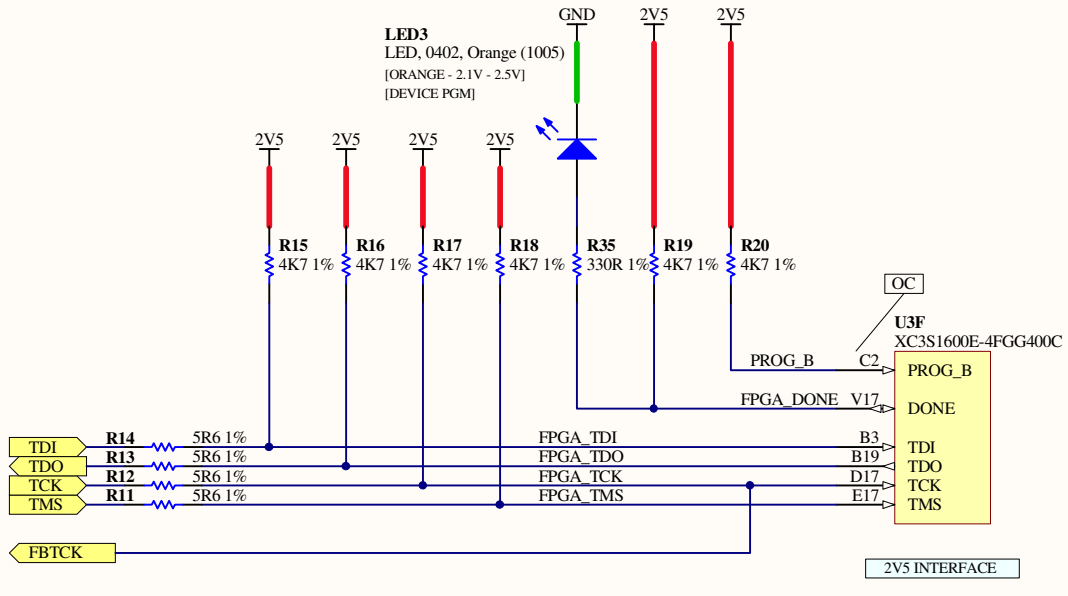
HSWAP (INT PULLED UP VIA FIXED RESISTOR) HSWAP HIGH - INT PULL UPS OFF HSWAP LOW - EXT PULL UPS ON (UG312-P37)

[HSWAP] HSWAP = L EXTERNAL PULL DOWN TO ENABLE PULL UP RESISTORS ON ALL IO

INTERNAL XC6SLX1600E RESISTANCE VALUES RPU - PULL UP RESISTOR (VCCO = 3V) = 100K OHMS RPD - PULL DOWN RESISTOR (VCCO = 3V) = 34K5 OHMS

M0, M1, M2 SET EXTERNAL SPI MASTER BOOT FROM EXTERNAL SPI FLASH

M0 = H EXTERNAL PULL UP
M1 = L EXTERNAL PULL DOWN
M2 = L EXTERNAL PULL DOWN (UG312-P34)

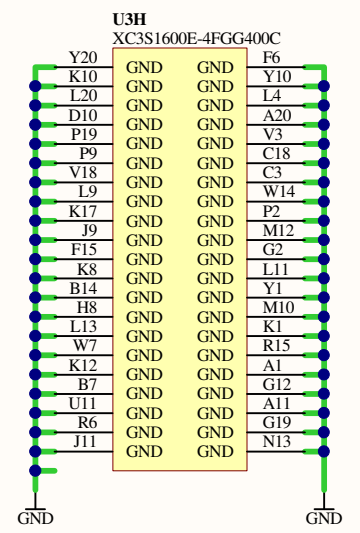
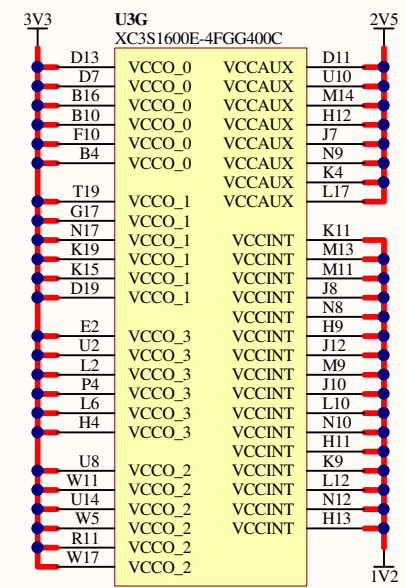


TDI, TDO, TCK AND TMS ALL REQUIRE SERIES RESISTOR FOR 3.3V OPERATION (XAPP453-P13)

FPGA_DONE PIN
H = PROGRAMMED (LOADED)
INTERNAL PULL UP
LOW BY DEFAULT

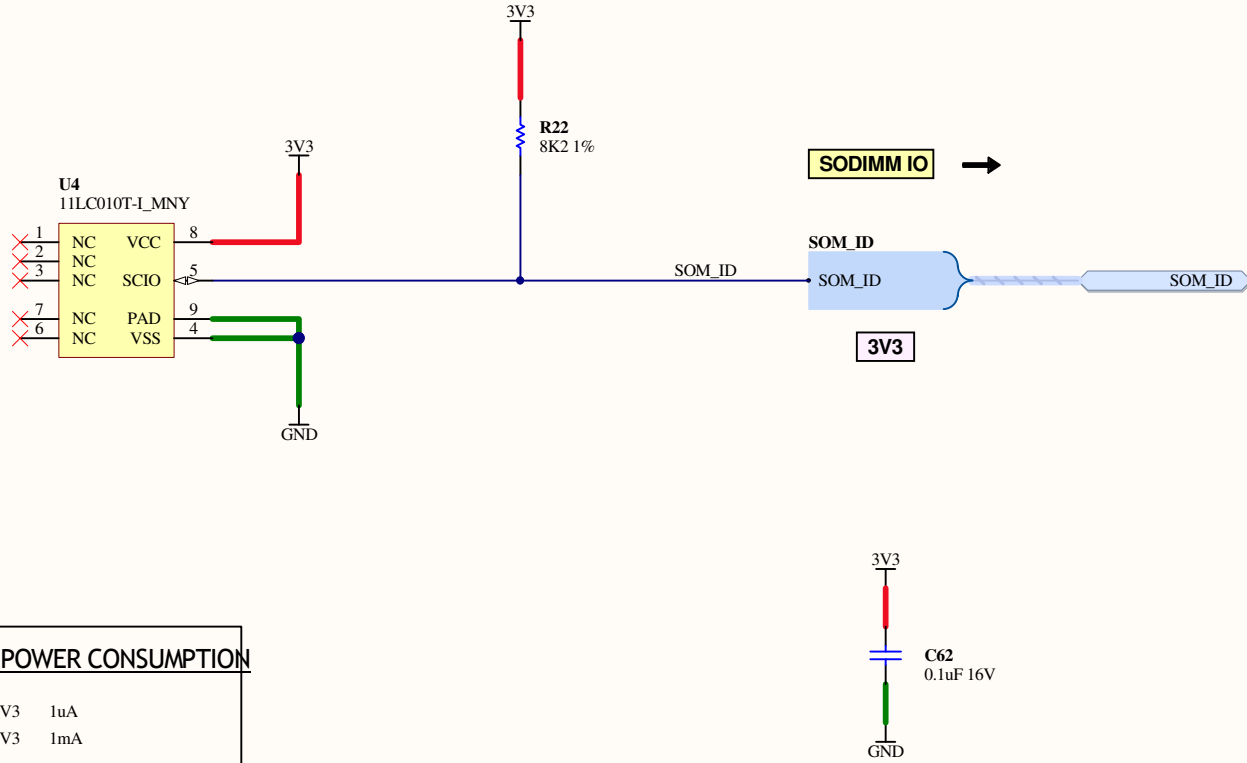
PROG_B (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
TO ALLOW CONFIGURATION TO START

DONE (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
HIGH = PROGRAM SUCCESSFUL



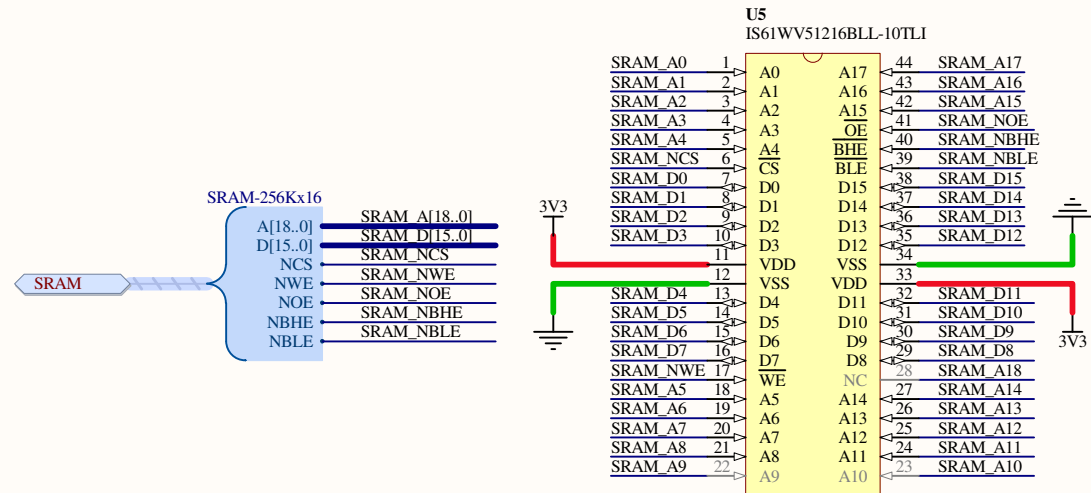
Sheet Title HOST FPGA Pwr and Programming			Altium Limited 3 Minna Close Belrose NSW 2085 Australia
Project Title SOM02			
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 7 of 13	
File: FPGA_NonIO.SchDoc			





11LC010T-L_MNY POWER CONSUMPTION		
STANDBY:	3V3	1uA
ACTIVE:	3V3	1mA

Title		
Size A4	Number	Revision
Date:	23/09/2011	Sheet of
File:	CASRKH\SOM03 - XC3S1600E\SOM_ID_Schematic By:	



IS61WV25616BLS FAST SRAM (10nS)
 256K x16 BITS 512K bytes

DEFAULT
 IS61WV51216BLL-10TLI FAST SRAM (10nS)
 512K x16 BITS 1M bytes

IS61WV20488BLL-10TLI FAST SRAM (10nS)
 2048K x8 BITS 2M bytes



Sheet Title 256K x 16-Bit SRAM		Altium Limited 3 Minna Close Belrose NSW 2085 Australia		
Project Title SOM02				
Size: A4	Assy: TBA			Revision: 04
Date: 23/09/2011	Time: 1:27:40 PM			Sheet 9 of 0
File: SRAM_512Kx16_TSOP44.SchDoc				

1

2

3

4

A

A

B

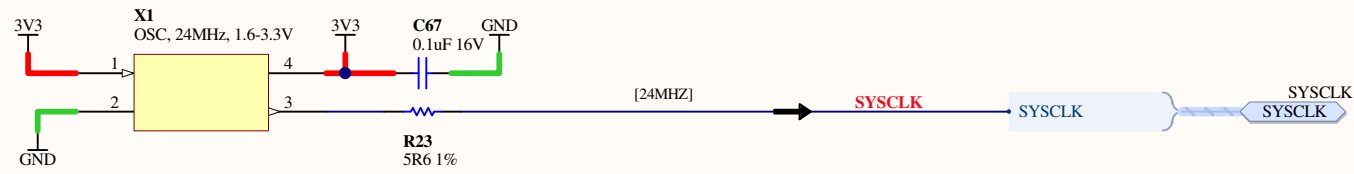
B


C

C

D

D



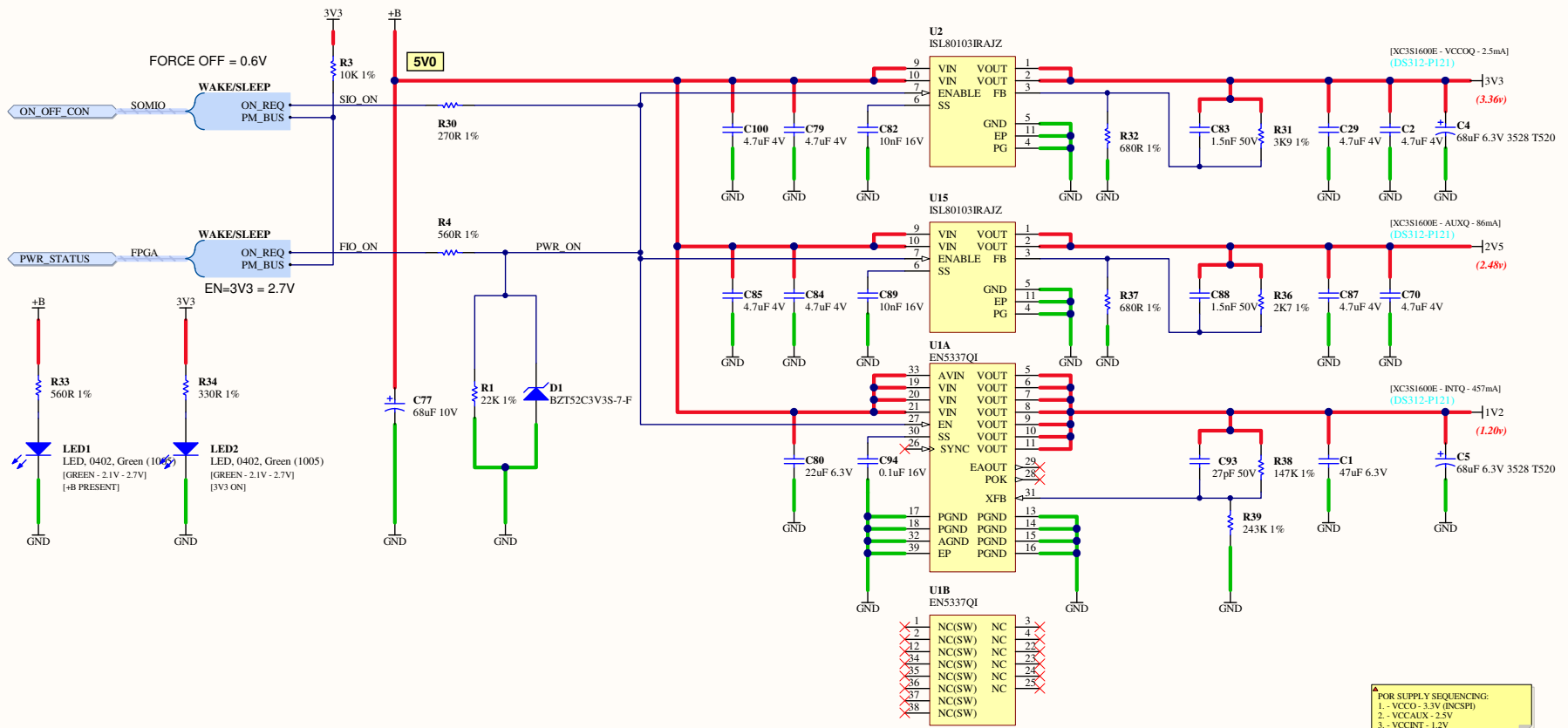
Sheet Title		16M x 32 SDRAM TSOP54 x 2		<i>Altium Limited</i> 3 Minna Close Belrose NSW 2085 Australia			
Project Title		SOM02					
Size:	A4	Assy:	TBA			Revision:	04
Date:	23/09/2011	Time:	1:27:40 PM			Sheet	10 of 13
File:		SYS_CLK.SchDoc					

1

2

3

4



A

B

C

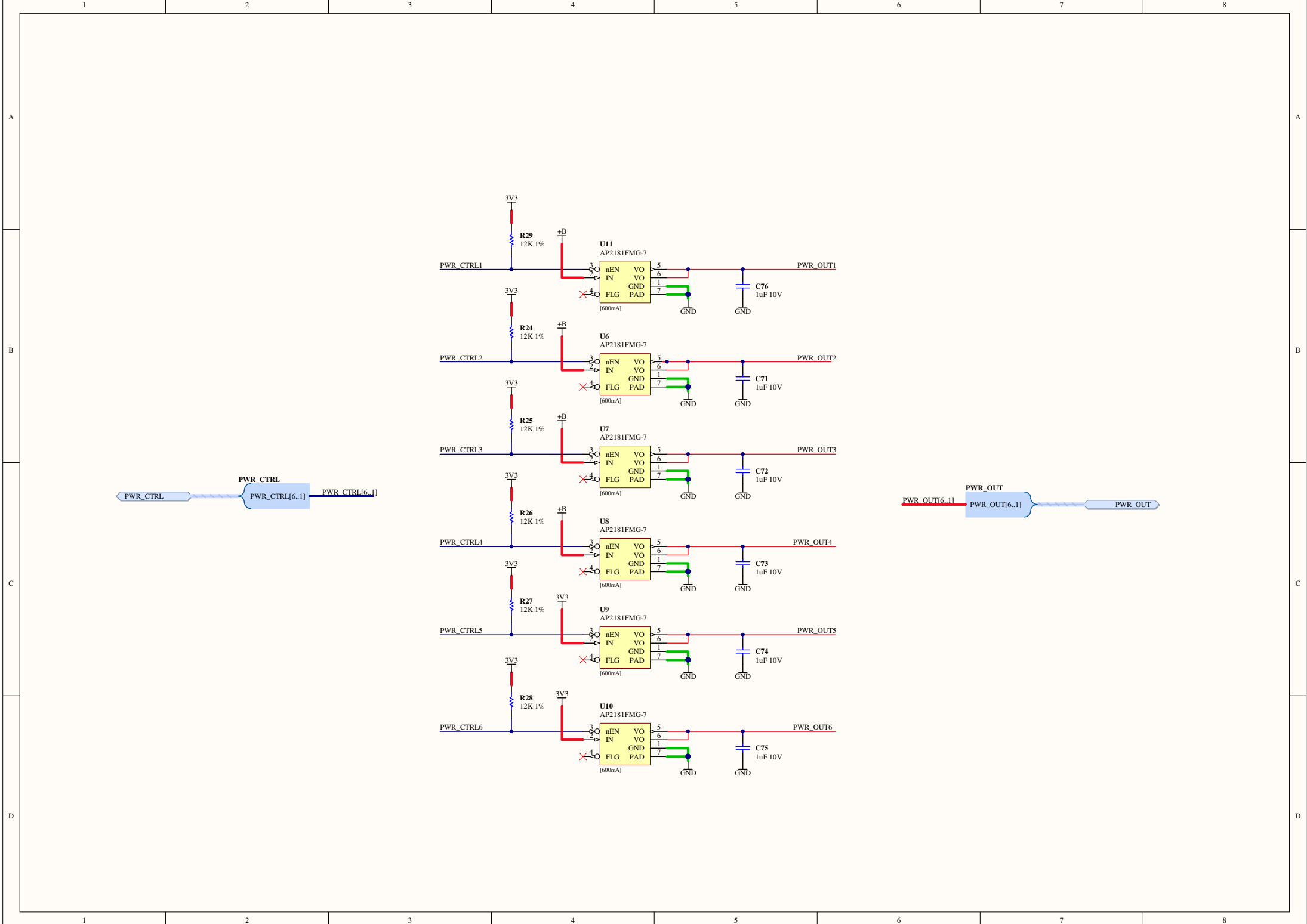
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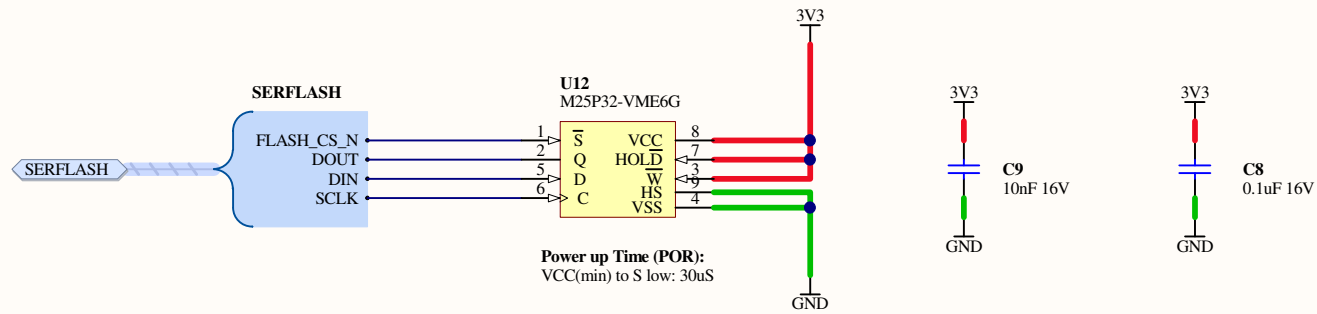
A

B

C

D





DEFAULT

M25P32-VME6G 32Mbit Serial PROM(75MHz)

33,554,432 BITS 4M bytes

(ID=0x2016)

M25P64-VME6G 64Mbit Serial PROM(75MHz)

67,108,864 BITS 8M bytes

(ID=0x2017)

M25P128-VME6G 128Mbit Serial PROM(54MHz)

134,217,728 BITS 16M bytes

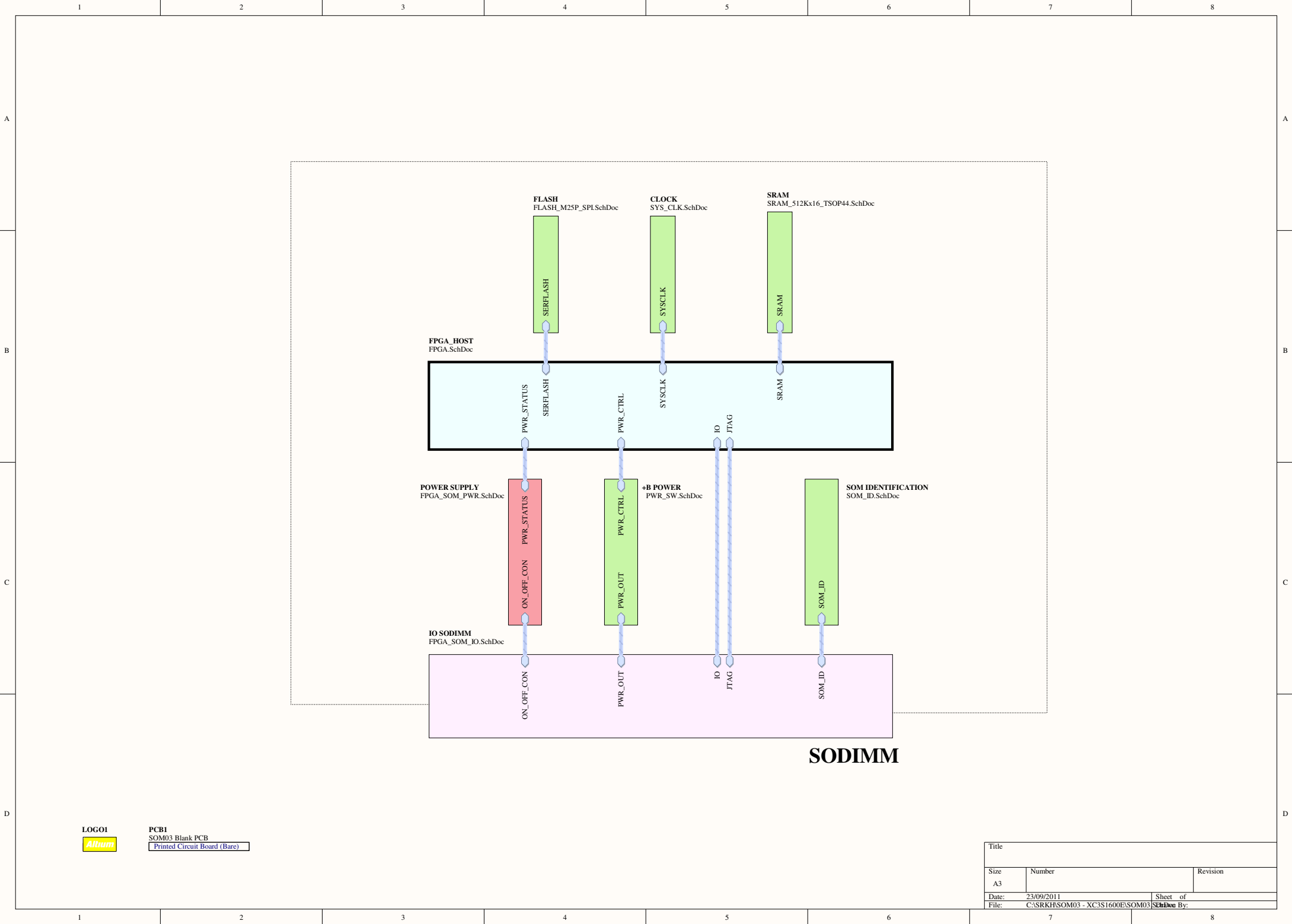
(ID=0x2018)

W25Q256FV 256Mbit Serial PROM (80MHz)

268,435,456 BITS 32M bytes

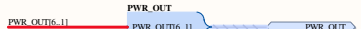
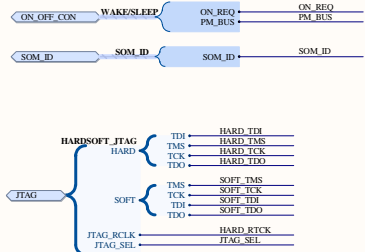
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Sheet Title Host - Dual Serial Flash Memory		Altium Limited 3 Minna Close Belrose NSW 2085 Australia	
Project Title SOM02			
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 13 of 13	
File: FLASH_M25P_SPI.SchDoc			



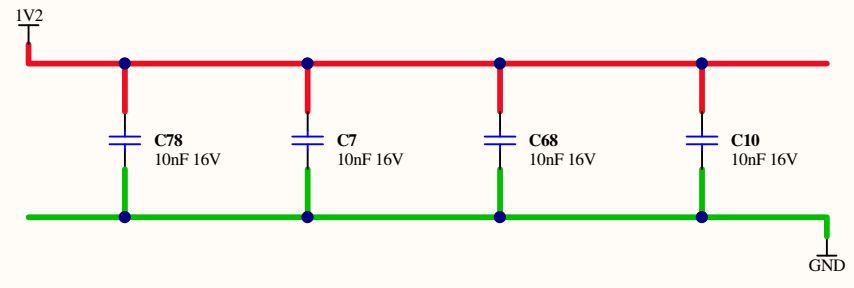
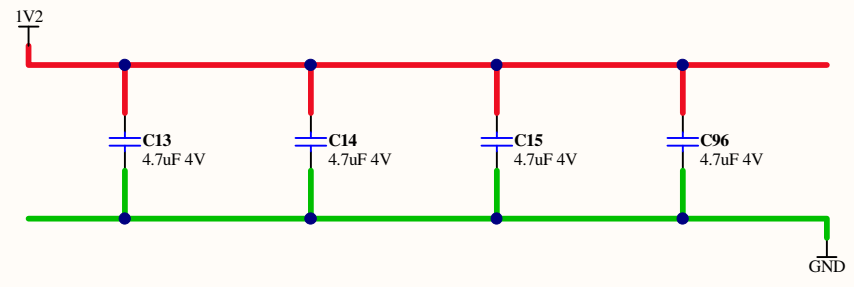
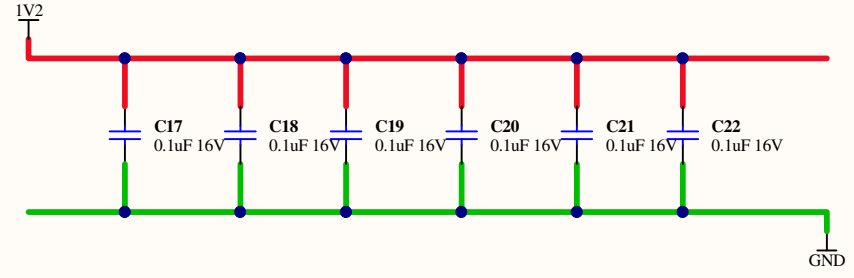
PCB1
SOM03 Blank PCB
Printed Circuit Board (Bare)


Title		
Size	Number	Revision
A3		
Date:	23/09/2011	Sheet of
File:	C:\SRKHSOM03 - XC3S1600E\SOM03	SchDoc By:

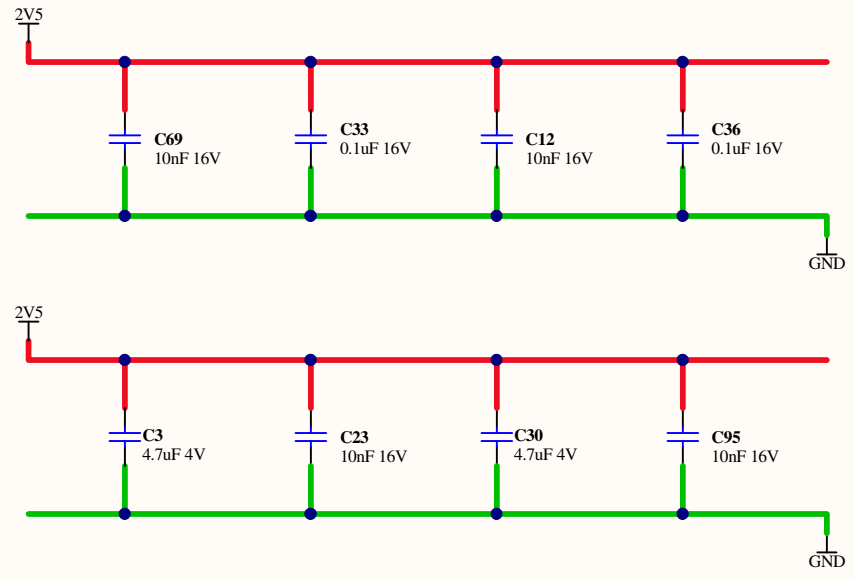



- JTAG
- SOM ID
- POWER ON
- GIGABIT ENET
- USB2 - PORT 1
- USB OTG
- SMB/PM BUS
- UART - PORT 1
- SPI - PORT 1
- SPI - PORT 2
- AHB CPU BUS
- SD CARD - PORT 1
- SD CARD - PORT 2
- SE VIDEO DATA
- DPDVI VIDEO

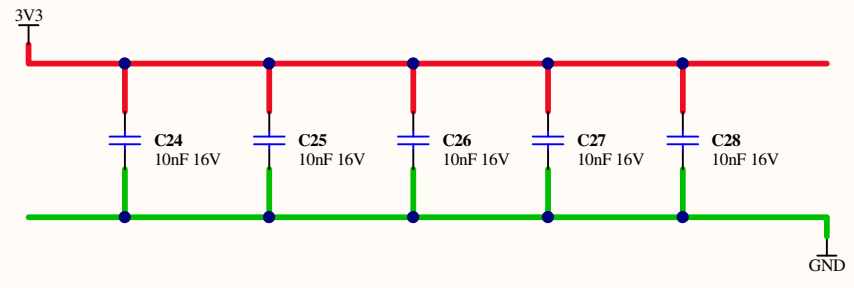
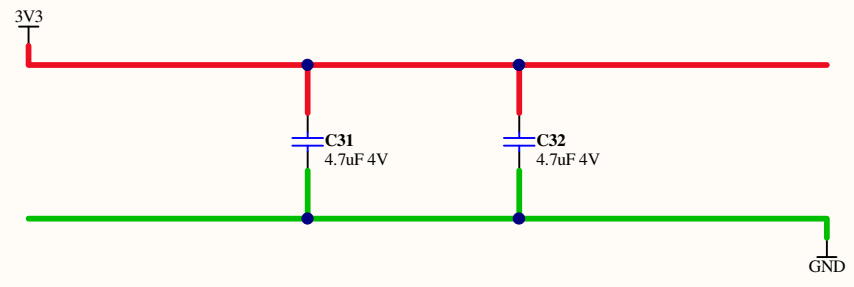
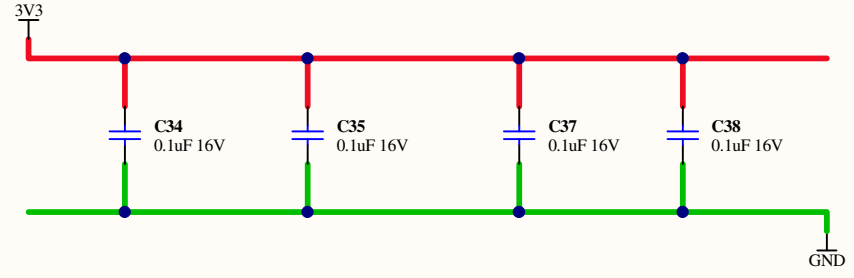
CNI		TOP		BOTTOM		CNI	
FPGA		COMP SIDE		SOLDER SIDE		FPGA	
JTAG_TDI	HARD_TDI	1	JTAG_TDI	2	HARD_TDI	JTAG_TDO	JTAG_TDO
JTAG_TCK	HARD_TCK	4	JTAG_TCK	5	HARD_TCK	JTAG_RTCK	JTAG_RTCK
SOM_ID	ON_REQ	7	MODULE_ID	6	JTAG_SEL	JTAG_SEL	JTAG_SEL
ON_REQ	ON_REQ	8	MOD_WAKE	7	GND	GND	GND
GND	GND	9	GND	8	GND	GND	GND
ENET_Ap	FPGA_I01	10	FPGA_I0p	10	FPGA_I0p	ENET_Bp	ENET_Bp
ENET_As	FPGA_I02	11	FPGA_I0s	11	FPGA_I0s	ENET_Bs	ENET_Bs
GND	GND	12	GND	12	GND	ENET_Dp	ENET_Dp
ENET_Cp	FPGA_I03	13	FPGA_I0c	13	FPGA_I0c	ENET_Ds	ENET_Ds
ENET-Cs	FPGA_I04	14	FPGA_I0c	14	FPGA_I0c	GND	GND
GND	GND	15	GND	15	GND	GND	GND
+B	GND	16	GND	16	GND	+B	+B
+B	GND	17	GND	17	GND	+B	+B
USB2_1_VBUS	PWR_OUT11	18	PWR_SW	18	PWR_SW	USB2_2_VBUS	USB2_2_VBUS
USB2_1_DP	PWR_OUT10	19	PWR_SW	19	PWR_SW	USB2_2_DM	USB2_2_DM
USB2_1_Dn	FPGA_I0p	20	FPGA_I0p	20	FPGA_I0p	USB2_2_Dp	USB2_2_Dp
GND	FPGA_I0n	21	FPGA_I0n	21	FPGA_I0n	GND	GND
USBOTG_Dp	GND	22	GND	22	GND	USB2_3_Dp	USB2_3_Dp
USBOTG_Ds	FPGA_I01	23	FPGA_I0p	23	FPGA_I0p	USB2_3_Ds	USB2_3_Ds
USBOTG_VBUS	FPGA_I014	24	FPGA_I0s	24	FPGA_I0s	USB2_1_VBUS	USB2_1_VBUS
USBOTG_VBUS	PWR_OUT13	25	PWR_SW	25	PWR_SW	USB2_3_VBUS	USB2_3_VBUS
USBOTG_ID	PWR_OUT12	26	PWR_SW	26	PWR_SW	GND	GND
PM_BUS	FPGA_I015	27	PM_BUS	27	PM_BUS	SDA	SDA
UART1_TXD	SOFT_TDO	28	SOFT_TDO	28	SOFT_TDO	SEL	SEL
UART1_RTS	SOFT_TMS	29	SOFT_TMS	29	SOFT_TMS	UART2_TXD	UART2_TXD
UART1_RXD	SOFT_TMS	30	SOFT_TMS	30	SOFT_TMS	UART2_RTS	UART2_RTS
UART1_CTS	SOFT_TDI	31	SOFT_TDI	31	SOFT_TDI	UART2_CTS	UART2_CTS
GND	SOFT_TCK	32	SOFT_TCK	32	SOFT_TCK	GND	GND
SPI1_TXD	GND	33	GND	33	GND	I2S_CS	I2S_CS
SPI1_RXD	FPGA_I04	34	FPGA_I0d	34	FPGA_I0d	I2S_CDOU1	I2S_CDOU1
SPI1_CLK	FPGA_I025	35	FPGA_I0k	35	FPGA_I0k	I2S_CCLK	I2S_CCLK
SPI1_CS	FPGA_I026	36	FPGA_I0k	36	FPGA_I0k	I2S_CDBN	I2S_CDBN
SPI2_TXD	FPGA_I027	37	FPGA_I0k	37	FPGA_I0k	I2S_LNCLK	I2S_LNCLK
SPI2_RXD	FPGA_I032	38	FPGA_I0d	38	FPGA_I0d	I2S_SECLK	I2S_SECLK
SPI2_CLK	FPGA_I031	39	FPGA_I0d	39	FPGA_I0d	I2S_SDBN	I2S_SDBN
SPI2_CS	FPGA_I034	40	FPGA_I0k	40	FPGA_I0k	I2S_SDOU1	I2S_SDOU1
GND	FPGA_I035	41	FPGA_I0k	41	FPGA_I0k	GND	GND
+B	GND	42	GND	42	GND	+B	+B
+B	GND	43	GND	43	GND	+B	+B
+B	GND	44	GND	44	GND	+B	+B
BUS_A0	FPGA_I040	45	FPGA_I0d	45	FPGA_I0d	BUS_D0	BUS_D0
BUS_A1	FPGA_I041	46	FPGA_I0d	46	FPGA_I0d	BUS_D1	BUS_D1
BUS_A2	FPGA_I042	47	FPGA_I0d	47	FPGA_I0d	BUS_D2	BUS_D2
BUS_A3	FPGA_I043	48	FPGA_I0d	48	FPGA_I0d	BUS_D3	BUS_D3
BUS_A4	FPGA_I044	49	FPGA_I0d	49	FPGA_I0d	BUS_D4	BUS_D4
BUS_A5	FPGA_I045	50	FPGA_I0d	50	FPGA_I0d	BUS_D5	BUS_D5
BUS_A6	FPGA_I046	51	FPGA_I0d	51	FPGA_I0d	BUS_D6	BUS_D6
BUS_A7	FPGA_I047	52	FPGA_I0d	52	FPGA_I0d	BUS_D7	BUS_D7
+B	FPGA_I047	53	FPGA_I0d	53	FPGA_I0d	+B	+B
BUS_A8	+B	54	+B	54	+B	BUS_D8	BUS_D8
BUS_A9	FPGA_I048	55	FPGA_I0d	55	FPGA_I0d	BUS_D9	BUS_D9
BUS_A10	FPGA_I049	56	FPGA_I0d	56	FPGA_I0d	BUS_D10	BUS_D10
BUS_A11	FPGA_I050	57	FPGA_I0d	57	FPGA_I0d	BUS_D11	BUS_D11
BUS_A12	FPGA_I051	58	FPGA_I0d	58	FPGA_I0d	BUS_D12	BUS_D12
BUS_A13	FPGA_I052	59	FPGA_I0d	59	FPGA_I0d	BUS_D13	BUS_D13
BUS_A14	FPGA_I053	60	FPGA_I0d	60	FPGA_I0d	BUS_D14	BUS_D14
BUS_A15	FPGA_I054	61	FPGA_I0d	61	FPGA_I0d	BUS_D15	BUS_D15
GND	FPGA_I055	62	FPGA_I0d	62	FPGA_I0d	GND	GND
BUS_A16	GND	63	GND	63	GND	BUS_CSD	BUS_CSD
BUS_A17	FPGA_I056	64	FPGA_I0d	64	FPGA_I0d	BUS_CSH	BUS_CSH
BUS_A18	FPGA_I057	65	FPGA_I0d	65	FPGA_I0d	BUS_CSD2	BUS_CSD2
BUS_A19	FPGA_I058	66	FPGA_I0d	66	FPGA_I0d	BUS_INT0	BUS_INT0
BUS_DMACK	FPGA_I059	67	FPGA_I0d	67	FPGA_I0d	BUS_INT1	BUS_INT1
BUS_DMARQ	FPGA_I061	68	FPGA_I0d	68	FPGA_I0d	BUS_AWE	BUS_AWE
BUS_AADV	FPGA_I062	69	FPGA_I0d	69	FPGA_I0d	BUS_WAIT	BUS_WAIT
BUS_AOE	FPGA_I063	70	FPGA_I0d	70	FPGA_I0d	BUS_CLK	BUS_CLK
+B	FPGA_I064	71	FPGA_I0d	71	FPGA_I0d	+B	+B
+B	FPGA_I064	72	FPGA_I0d	72	FPGA_I0d	+B	+B
+B	FPGA_I064	73	FPGA_I0d	73	FPGA_I0d	+B	+B
FXD0ANK	FPGA_I066	74	FPGA_I0d	74	FPGA_I0d	SD1_DAT0	SD1_DAT0
PXD0AT0	FPGA_I068	75	FPGA_I0d	75	FPGA_I0d	SD1_DAT1	SD1_DAT1
PXD0AT1	FPGA_I069	76	FPGA_I0d	76	FPGA_I0d	SD1_DAT2	SD1_DAT2
PXD0AT2	FPGA_I070	77	FPGA_I0d	77	FPGA_I0d	SD1_DAT3	SD1_DAT3
PXD0AT3	FPGA_I071	78	FPGA_I0d	78	FPGA_I0d	SD1_CMD	SD1_CMD
PXD0AT4	FPGA_I072	79	FPGA_I0d	79	FPGA_I0d	SD1_CLK	SD1_CLK
PXD0AT5	FPGA_I073	80	FPGA_I0d	80	FPGA_I0d	SD1_CD	SD1_CD
PXD0AT6	FPGA_I074	81	FPGA_I0d	81	FPGA_I0d	SD1_PWR	SD1_PWR
PXD0AT7	FPGA_I075	82	FPGA_I0d	82	FPGA_I0d	SD2_DAT0	SD2_DAT0
PXD0AT8	FPGA_I076	83	FPGA_I0d	83	FPGA_I0d	SD2_DAT1	SD2_DAT1
PXD0AT9	FPGA_I077	84	FPGA_I0d	84	FPGA_I0d	SD2_DAT2	SD2_DAT2
PXD0AT10	FPGA_I078	85	FPGA_I0d	85	FPGA_I0d	SD2_DAT3	SD2_DAT3
PXD0AT11	FPGA_I079	86	FPGA_I0d	86	FPGA_I0d	SD2_CMD	SD2_CMD
PXD0AT12	FPGA_I080	87	FPGA_I0d	87	FPGA_I0d	SD2_CLK	SD2_CLK
PXD0AT13	FPGA_I081	88	FPGA_I0d	88	FPGA_I0d	SD2_CD	SD2_CD
PXD0AT14	FPGA_I082	89	FPGA_I0d	89	FPGA_I0d	SD2_PWR	SD2_PWR
PXD0AT15	FPGA_I083	90	FPGA_I0d	90	FPGA_I0d	DPDVI_HPD	DPDVI_HPD
PXD0AT16	FPGA_I084	91	FPGA_I0d	91	FPGA_I0d	DPDVI_CLK	DPDVI_CLK
PXD0AT17	FPGA_I085	92	FPGA_I0d	92	FPGA_I0d	DPDVI_n_DAT	DPDVI_n_DAT
PXD0AT18	FPGA_I086	93	FPGA_I0d	93	FPGA_I0d	GND	GND
PXD0AT19	FPGA_I087	94	FPGA_I0d	94	FPGA_I0d	DPDVI_p0	DPDVI_p0
PXD0AT20	FPGA_I088	95	FPGA_I0d	95	FPGA_I0d	DPDVI_n0	DPDVI_n0
PXD0AT21	FPGA_I089	96	FPGA_I0d	96	FPGA_I0d	GND	GND
PXD0AT22	FPGA_I090	97	FPGA_I0d	97	FPGA_I0d	DPDVI_p1	DPDVI_p1
PXD0AT23	FPGA_I091	98	FPGA_I0d	98	FPGA_I0d	GND	GND
PDCLK	FPGA_I012	99	FPGA_I0d	99	FPGA_I0d	DPDVI_p2	DPDVI_p2
PMHS	FPGA_I013	100	FPGA_I0k	100	FPGA_I0k	GND	GND
PMVS	FPGA_I014	101	FPGA_I0k	101	FPGA_I0k	DPDVI_n2	DPDVI_n2
+B	FPGA_I015	102	FPGA_I0d	102	FPGA_I0d	GND	GND
+B	FPGA_I015	103	FPGA_I0d	103	FPGA_I0d	DPDVI_CLKp	DPDVI_CLKp
+B	FPGA_I015	104	FPGA_I0d	104	FPGA_I0d	DPDVI_CLKn	DPDVI_CLKn
+B1	FPGA_I015	105	FPGA_I0d	105	FPGA_I0d	GND	GND
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+B1	FPGA_I015	126	FPGA_I0d	126	FPGA_I0d	GND	GND
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+B1	FPGA_I015	135	FPGA_I0d	135	FPGA_I0d	GND	GND
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+B1	FPGA_I015	137	FPGA_I0d	137	FPGA_I0d	GND	GND
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+B1	FPGA_I015	147	FPGA_I0d	147	FPGA_I0d	GND	GND
+B1	FPGA_I015	148	FPGA_I0d	148	FPGA_I0d	GND	GND
+B1	FPGA_I015	149	FPGA_I0d	149	FPGA_I0d	GND	GND
+B1	FPGA_I015	150	FPGA_I0d	150	FPGA_I0d	GND	GND
+B1	FPGA_I015	151	FPGA_I0d	151	FPGA_I0d	GND	GND
+B1	FPGA_I015	152	FPGA_I0d	152	FPGA_I0d	GND	GND
+B1	FPGA_I015	153	FPGA_I0d	153	FPGA_I0d	GND	GND
+B1	FPGA_I015	154	FPGA_I0d	154	FPGA_I0d	GND	GND
+B1	FPGA_I015	155	FPGA_I0d	155	FPGA_I0d	GND	GND
+B1	FPGA_I015	156	FPGA_I0d	156	FPGA_I0d	GND	GND
+B1	FPGA_I015	157	FPGA_I0d	157	FPGA_I0d	GND	GND
+B1	FPGA_I015	158	FPGA_I0d	158	FPGA_I0d	GND	GND
+B1	FPGA_I015	159	FPGA_I0d	159	FPGA_I0d	GND	GND
+B1	FPGA_I015	160	FPGA_I0d	160	FPGA_I0d	GND	GND
+B1	FPGA_I015	161	FPGA_I0d	161	FPGA_I0d	GND	GND
+B1	FPGA_I015	162	FPGA_I0d	162	FPGA_I0d	GND	GND
+B1	FPGA_I015	163	FPGA_I0d	163	FPGA_I0d	GND	GND
+B1	FPGA_I015	164	FPGA_I0d	164	FPGA_I0d	GND	GND
+B1	FPGA_I015	165	FPGA_I0d	165	FPGA_I0d	GND	GND
+B1	FPGA_I015	166	FPGA_I0d	166	FPGA_I0d	GND	GND
+B1	FPGA_I015	167	FPGA_I0d	167	FPGA_I0d	GND	GND
+B1	FPGA_I015	168	FPGA_I0d	168	FPGA_I0d	GND	GND
+B1	FPGA_I015	169	FPGA_I0d	169	FPGA_I0d	GND	GND
+B1	FPGA_I015	170	FPGA_I0d	170	FPGA_I0d	GND	GND
+B1	FPGA_I015	171	FPGA_I0d	171	FPGA_I0d	GND	GND
+B1	FPGA_I015	172	FPGA_I0d	172	FPGA_I0d	GND	GND
+B1	FPGA_I015	173	FPGA_I0d	173	FPGA_I0d	GND	GND
+B1	FPGA_I015	174	FPGA_I0d	174	FPGA_I0d	GND	GND
+B1	FPGA_I015	175	FPGA_I0d	175	FPGA_I		



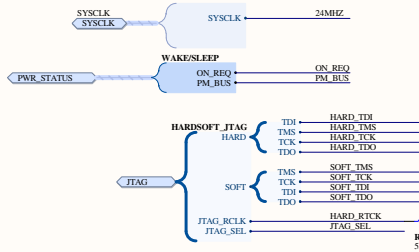
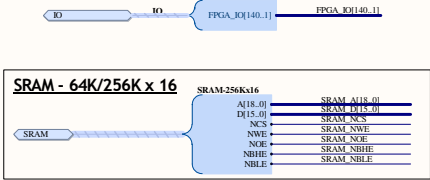
Sheet Title FPGA Bypass 2V5			Altium Limited 3 Minna Close Belrose NSW 2085 Australia	
Project Title SOM02				
Size: A4	Assy: TBA	Revision: 04		
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 3 of 13		
File: FPGA_Bypass_FPGA_1V2.SchDoc				



Sheet Title FPGA Bypass 2V5		Altium Limited 3 Minna Close Belrose NSW 2085 Australia	
Project Title SOM02			
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 4 of 13	
File: FPGA_Bypass_FPGA_2V5.SchDoc			

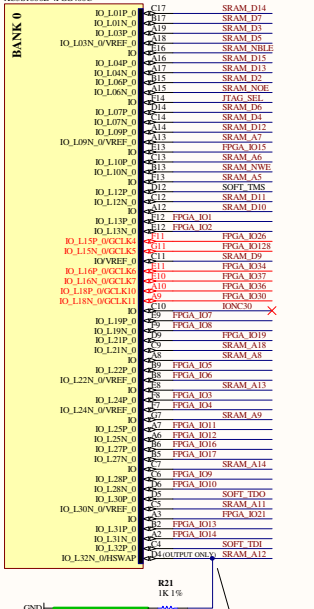


Sheet Title FPGA Bypass 2V5		Altium Limited 3 Minna Close Belrose NSW 2085 Australia	
Project Title SOM02			
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 5 of 13	
File: FPGA_Bypass_FPGA_3V3.SchDoc			



GCLK0
FPGA SYSTEM CLOCK IS ON GLOBAL CLOCK @ 24MHZ

U0A
XC6SLX1600E-4FGG400C

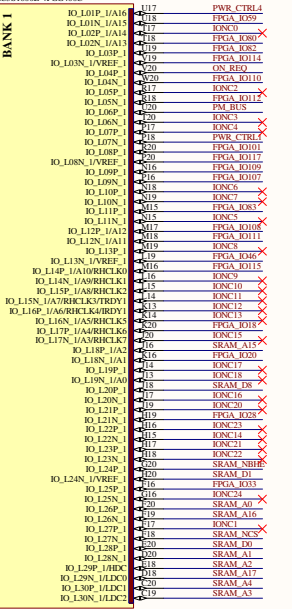


HSWAP (INT PULLED UP VIA FIXED RESISTOR)
HSWAP HIGH - INT PULLUPS OFF
HSWAP LOW - INT PULLUPS ON (UG312-P14)

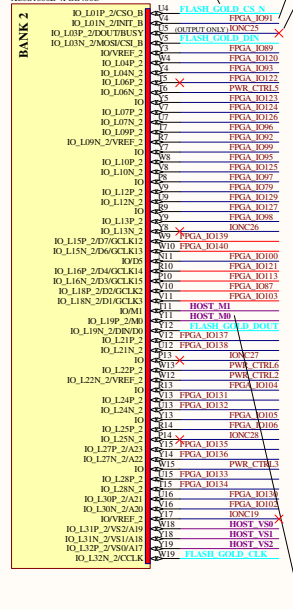
[HSWAP]
HSWAP = L
EXTERNAL PULL DOWN TO ENABLE PULL UP RESISTORS ON ALL IO

INTERNAL XC6SLX1600E RESISTANCE VALUES
RPU - PULL UP RESISTOR (VCC0 = 3V) = 100K OHMS
RPD - PULL DOWN RESISTOR (VCC0 = 3V) = 34K5 OHMS

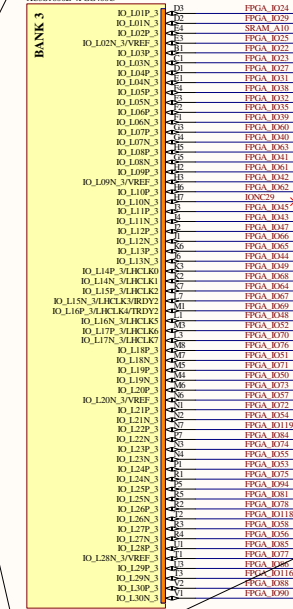
U0B
XC6SLX1600E-4FGG400C



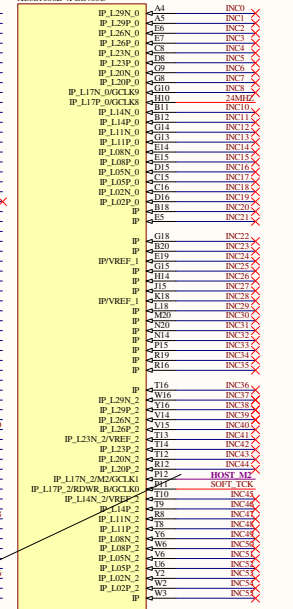
U0C
XC6SLX1600E-4FGG400C



U0D
XC6SLX1600E-4FGG400C



U0E
XC6SLX1600E-4FGG400C

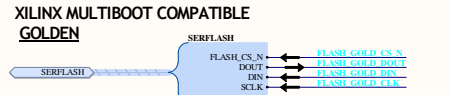


1V2
FPGA DECOUPLING CAPS 1V2
FPGA_Bypass_FPGA_1V2.SchDoc

2V5
FPGA DECOUPLING CAPS 2V5
FPGA_Bypass_FPGA_2V5.SchDoc

3V3
FPGA DECOUPLING CAPS 3V3
FPGA_Bypass_FPGA_3V3.SchDoc

NOTE:
INT B ASSERTS DURING CONFIG.
DOUT OSCILLATES DURING CONFIG.
FPGA WILL ATTEMPT SPI BOOT THREE TIMES (UG312-P127)



M0	M1	M2	FUNCTION
0	0	0	PLATFORM FLASH MODE
0	0	1	SPI MASTER (MASTER)
0	1	0	BYTE PARALLEL INTERFACE
0	1	1	INTERNAL MASTER SPI FLASH
1	0	0	<RESERVED>
1	0	1	JTAG MODE
1	1	0	SLAVE PARALLEL
1	1	1	SLAVE SERIAL

[M0]
M0 = H
INTERNAL PULL UP BY HSWAP PRIOR TO CONFIGURATION (UG312-P14) (UG312-P16)

V0S1	V0S2	FUNCTION
0	0	<RESERVED>
0	1	<RESERVED>
1	0	<RESERVED>
1	0	(000) STANDARD READ
1	1	(000) READ ARBITRARY
1	1	(000) SPI FAST READ

[M0] SPI MODE (MASTER)
HOST_M0 -> V3V3
HOST_M1 -> GND
HOST_M2 -> GND
HOST_M3 -> V3V3
HOST_V0 -> V3V3
HOST_V01 -> V3V3
HOST_V02 -> V3V3
HOST_V03 -> V3V3

M0 (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
EXT SPI BOOT MODE (MASTER)

M1 (INT PULL UP VIA HSWAP)
MUST BE PULLED LOW DURING CONFIG
EXT SPI BOOT MODE (MASTER)

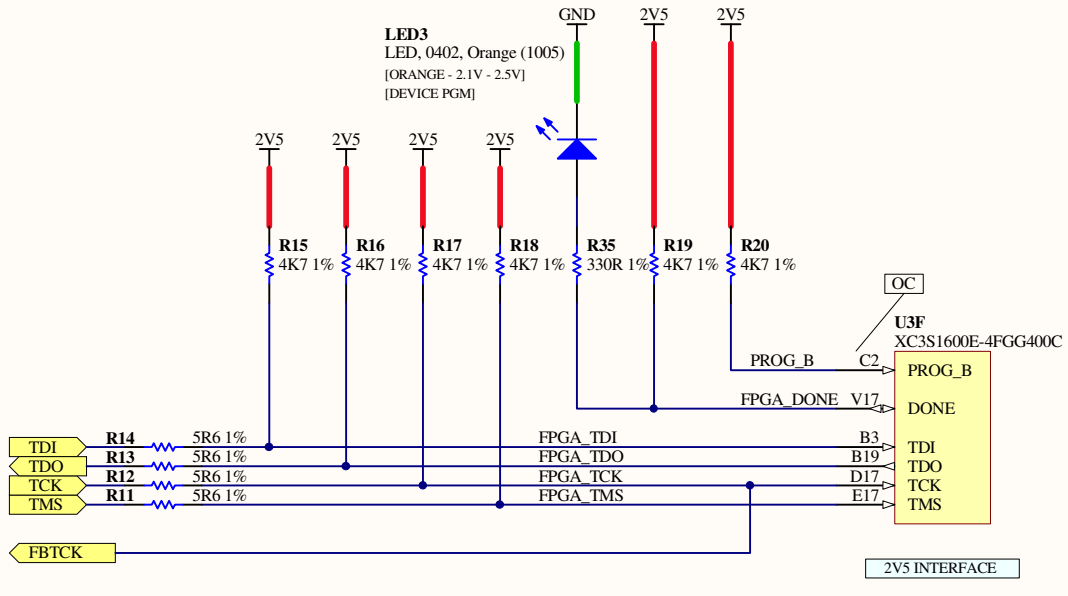
M2 (INT PULL UP VIA HSWAP)
MUST BE PULLED LOW DURING CONFIG
EXT SPI BOOT MODE (MASTER)

V0S0 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (000) (VCC0)

V0S1 SPI ACCESS SPEED (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
SPI SET TO FAST (000) (VCC0)

Sheet Title: **Host Controller - Spartan3AN-400**
Project Title: **SOM2**
Size: A2 Assy: TBA Revision: 04
Date: 23/09/2011 Time: 1:27:40 PM Sheet 6 of 13
File: FPGA_SchDoc

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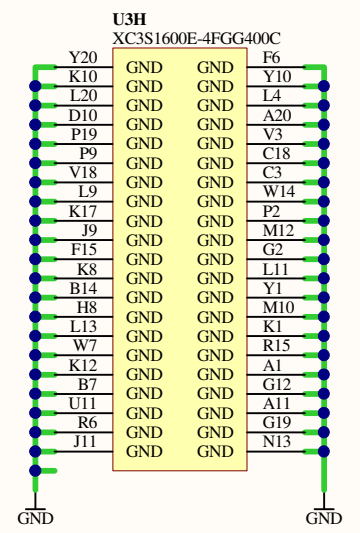
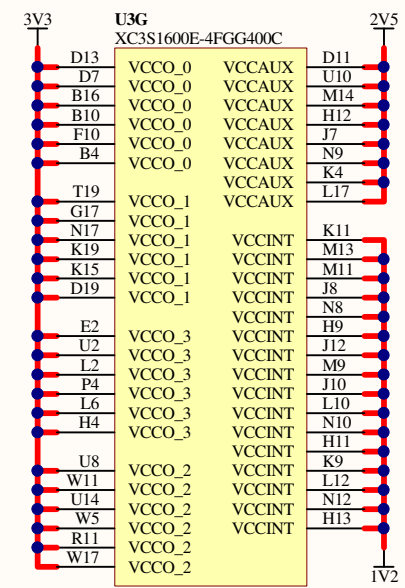


TDI, TDO, TCK AND TMS ALL REQUIRE SERIES RESISTOR FOR 3.3V OPERATION (XAPP453-P13)

FPGA_DONE PIN
H = PROGRAMMED (LOADED)
INTERNAL PULL UP
LOW BY DEFAULT

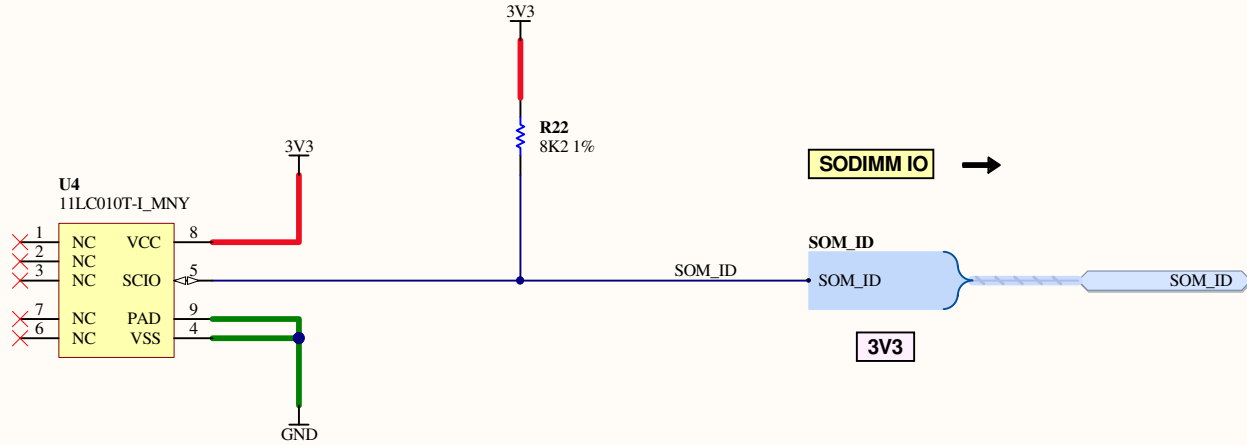
PROG_B (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
TO ALLOW CONFIGURATION TO START

DONE (INT PULL UP VIA HSWAP)
MUST BE PULLED HIGH DURING CONFIG
HIGH = PROGRAM SUCCESSFUL

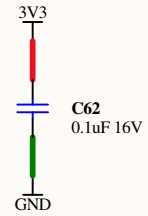


Sheet Title HOST FPGA Pwr and Programming			Altium Limited 3 Minna Close Belrose NSW 2085 Australia
Project Title SOM02			
Size: A4	Assy: TBA	Revision: 04	
Date: 23/09/2011	Time: 1:27:40 PM	Sheet 7 of 13	
File: FPGA_NonIO.SchDoc			

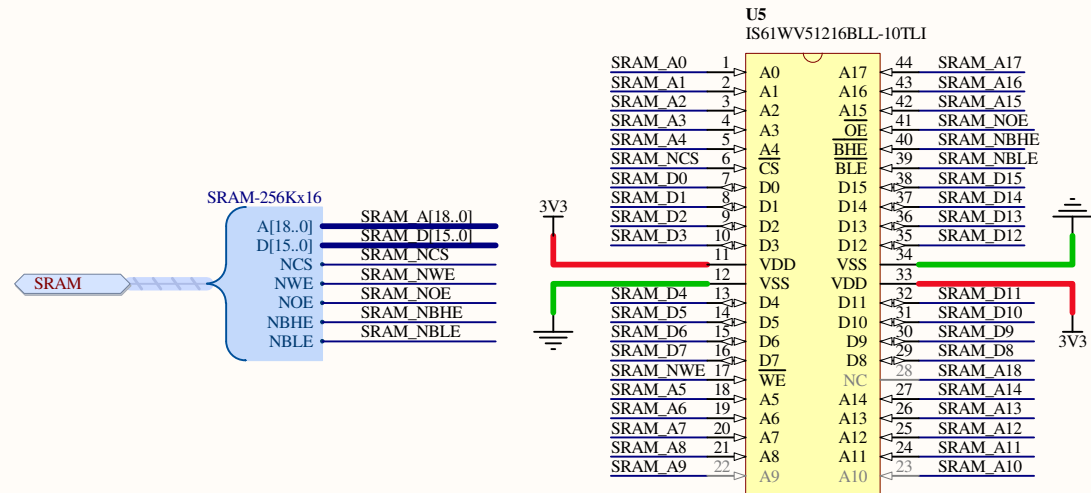




11LC010T-L_MNY POWER CONSUMPTION		
STANDBY:	3V3	1uA
ACTIVE:	3V3	1mA



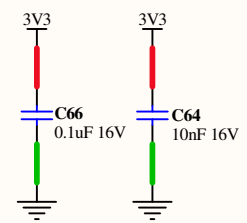
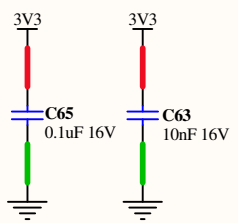
Title		
Size A4	Number	Revision
Date:	23/09/2011	Sheet of
File:	CASRKH\SOM03 - XC3S1600E\SOM_ID_Schematic By:	



IS61WV25616BLS FAST SRAM (10nS)
256K x16 BITS 512K bytes

DEFAULT
IS61WV51216BLL-10TLI FAST SRAM (10nS)
512K x16 BITS 1M bytes

IS61WV20488BLL-10TLI FAST SRAM (10nS)
2048K x8 BITS 2M bytes



Sheet Title 256K x 16-Bit SRAM		Altium Limited 3 Minna Close Belrose NSW 2085 Australia		
Project Title SOM02				
Size: A4	Assy: TBA			Revision: 04
Date: 23/09/2011	Time: 1:27:40 PM			Sheet 9 of 0
File: SRAM_512Kx16_TSOP44.SchDoc				

1

2

3

4

A

A

B

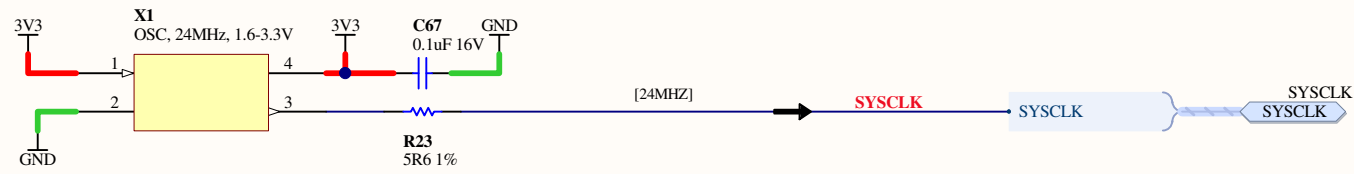
B


C

C

D

D



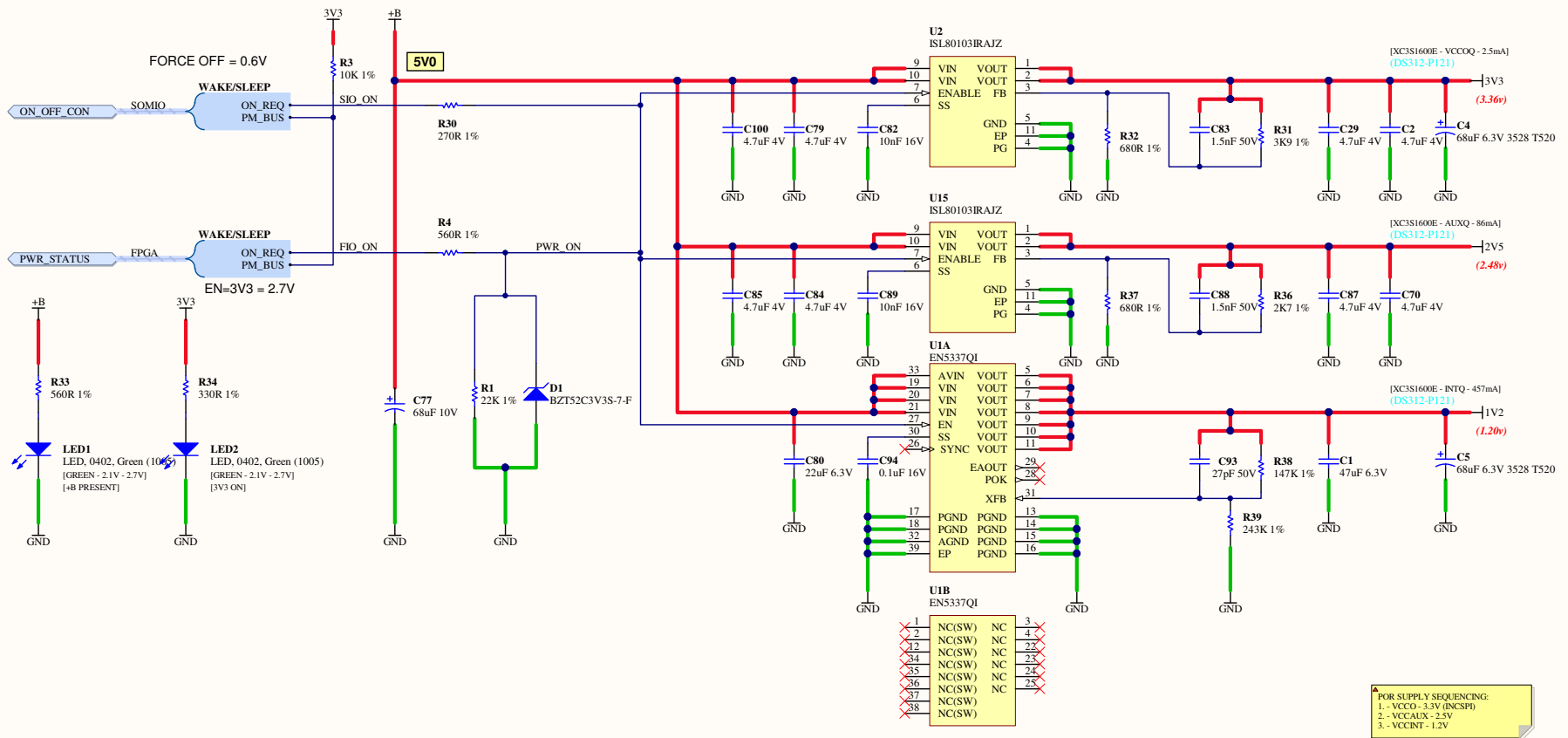
Sheet Title 16M x 32 SDRAM TSOP54 x 2		<i>Altium Limited</i> 3 Minna Close Belrose NSW 2085 Australia		
Project Title SOM02				
Size: A4	Assy: TBA			Revision: 04
Date: 23/09/2011	Time: 1:27:40 PM			Sheet 10 of 13
File: SYS_CLK.SchDoc				

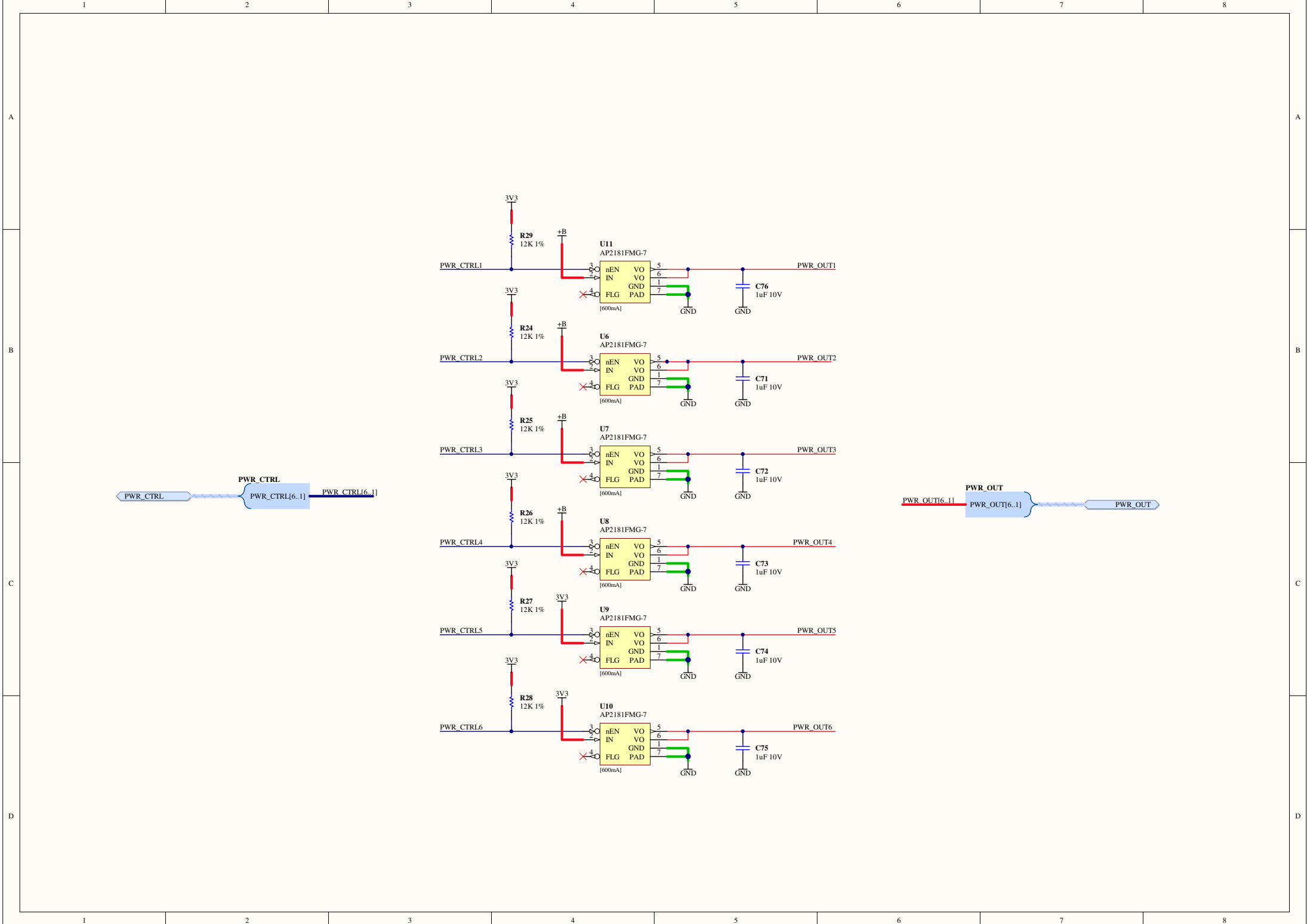
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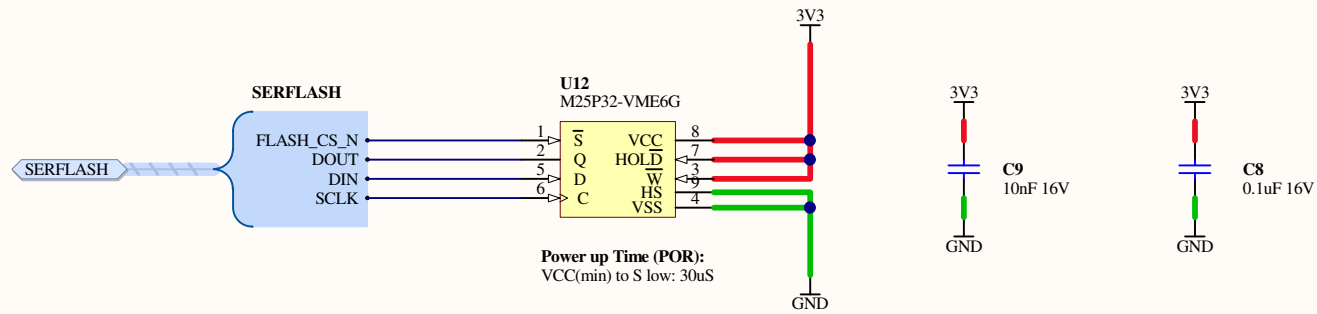
2

3

4







DEFAULT

M25P32-VME6G 32Mbit Serial PROM (75MHz)

33,554,432 BITS 4M bytes

(ID=0x2016)

M25P64-VME6G 64Mbit Serial PROM (75MHz)

67,108,864 BITS 8M bytes

(ID=0x2017)

M25P128-VME6G 128Mbit Serial PROM (54MHz)

134,217,728 BITS 16M bytes

(ID=0x2018)

W25Q256FV 256Mbit Serial PROM (80MHz)

268,435,456 BITS 32M bytes

(ID=0x4019)

Sheet Title *Host - Dual Serial Flash Memory*

Project Title *SOM02*

Size: A4

Assy: TBA

Revision: 04

Date: 23/09/2011 Time: 1:27:40 PM

Sheet 13 of 13

File: FLASH_M25P_SPI.SchDoc

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